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CROSS REFERENCE

This is a divisional application of the co-pending U.S. Patent Application Serial No. 09/450,333 filed on November 29, 1999, which has become U.S. Patent No. _____. –

In the Claims:

Please cancel claims 1-13 and 18-19 without any disclaimer and a prejudice to.

In the Abstract:

At the end of the claims please add the following paragraph starting as a new page.

ABSTRACT OF THE DISCLOSURE

A gate wire including a gate line extending in the horizontal direction, and a gate electrode is formed on an insulating substrate. A gate insulating layer is formed on the gate wire and covers the same. A semiconductor pattern is formed on the gate insulating layer 30, and formed on the semiconductor pattern are a data wire having a date line in the vertical direction, a source electrode, a drain electrode separated from the source electrode opposite the source electrode with respect to the gate electrode, and an align pattern located on both sides of the data line. A passivation layer is formed on the data wire and the align pattern, and has contact holes exposing the drain electrode and an opening exposing the substrate between the data line and the align pattern. Here, the align pattern adjacent to the data line is exposed through the opening, and the semiconductor pattern and the gate insulating layer are under-cut. A pixel electrode